Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**

**.035”**

**FD41401**

**MASK**

**REF**

**RF1**

**RF2**

**IF1**

**LO1**

**LO2**

**ESD**

**GND**

**IF2**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0033” X .0033”**

**Backside Potential: N/A**

**Mask Ref: FD41401**

**APPROVED BY: DK DIE SIZE .030” X .035” DATE: 5/22/17**

**MFG: PEREGRINE THICKNESS .007” P/N: PE4140**

**DG 10.1.2**

#### Rev B, 7/1